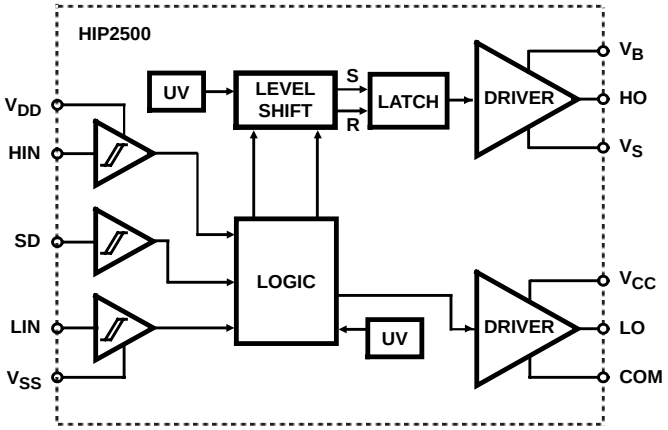
## General Description

The HIP2500 model utilizes macro modeling constructs to accurately simulate DC and transient effects. This model is composed entirely of standard SPICE elements (using standard SPICE code makes the macromodel portable to nearly all of the SPICE-derivative simulators on the market today). In order to properly capture the characteristics of the HIP2500, the architecture of this model maintains some correspondence to the actual circuitry. The input and output devices of the transistor circuit are copied in the model so as to reproduce the proper input loading and output drive capabilities. The logic functionality and related delay times are adequately modeled using a reduced count of logic functions constructed from polynomial dependent sources, resistors, capacitors and diodes. DC convergence of the model is quickly achieved because of an internal feedback limiting feature.

## Functional Block Diagram




## Netlist Syntax

The full HIP2500 model file must be included in the simulation netlist. Also, the following subcircuit call syntax must be used for each model occurrence in the design:

Xname Nvdd Nhin Nsd Nlin Nvss Nvb Nho Nvs Nvcc Nlo Ncom HIP2500

Where:

name-unique name for each HIP2500 occurrence in the schematic

Nxxx-design node number connected to the xxx pin of the HIP2500

## Notes

This model is only intended for use at nominal temperature.

Because the architecture of the model maintaines some correspondence with the actual circuitry, it is important to remember that the initial states on the internal logic sections will be random at the beginning of any transient simulation where the rail to rail supply voltages start within the recommended operating ranges. In this situation, the circuits built in power-up initialization feature is not activated, and it is possible for some simulations to appear as if the model is not working properly. The only way to guarantee the functional accuracy of this model with the actual circuit is to ramp up the rail to rail output supply voltages from below the data sheet undervoltage negative going threshold minimum up to within the recommended operating conditions at the beginning of each transient simulation. This way the internal states of the model will be properly initialized in the same manner as those on the actual chip.

## *Sales Office Headquarters*

**NORTH AMERICA**
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

**EUROPE**
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029